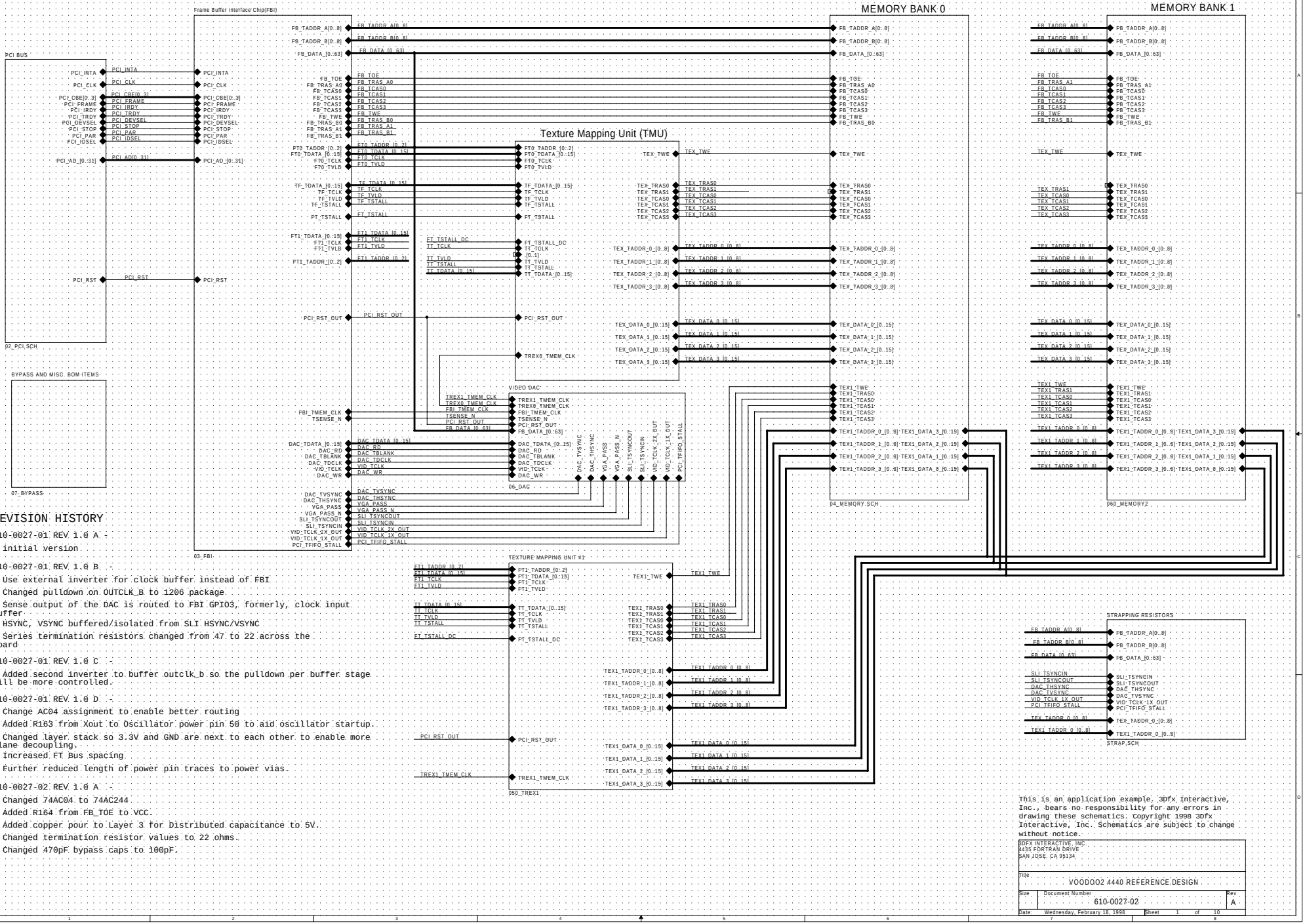
VOODOO-2 4440 REFERENCE DESIGN



REVISION HISTORY

610-0027-01 REV 1.0 A -

- initial version

610-0027-01 REV 1.0 B -

- Use external inverter for clock buffer instead of FBI
- Changed pulldown on OUTCLK_B to 1206 package
- Sense output of the DAC is routed to FBI GPIO3, formerly, clock input buffer
- HSYNC, VSYNC buffered/isolated from SLI HSYNC/VSYNC
- Series termination resistors changed from 47 to 22 across the board

610-0027-01 REV 1.0 C -

- Added second inverter to buffer outclk_b so the pulldown per buffer stage will be more controlled.

610-0027-01 REV 1.0 D -

- Change AC04 assignment to enable better routing
- Added R163 from Xout to Oscillator power pin 50 to aid oscillator startup.
- Changed layer stack so 3.3V and GND are next to each other to enable more plane decoupling.
- Increased FT Bus spacing
- Further reduced length of power pin traces to power vias.

610-0027-02 REV 1.0 A -

- Changed 74AC04 to 74AC244
- Added R164 from FB_TOE to VCC.
- Added copper pour to Layer 3 for Distributed capacitance to 5V.
- Changed termination resistor values to 22 ohms.
- Changed 470pF bypass caps to 100pF.

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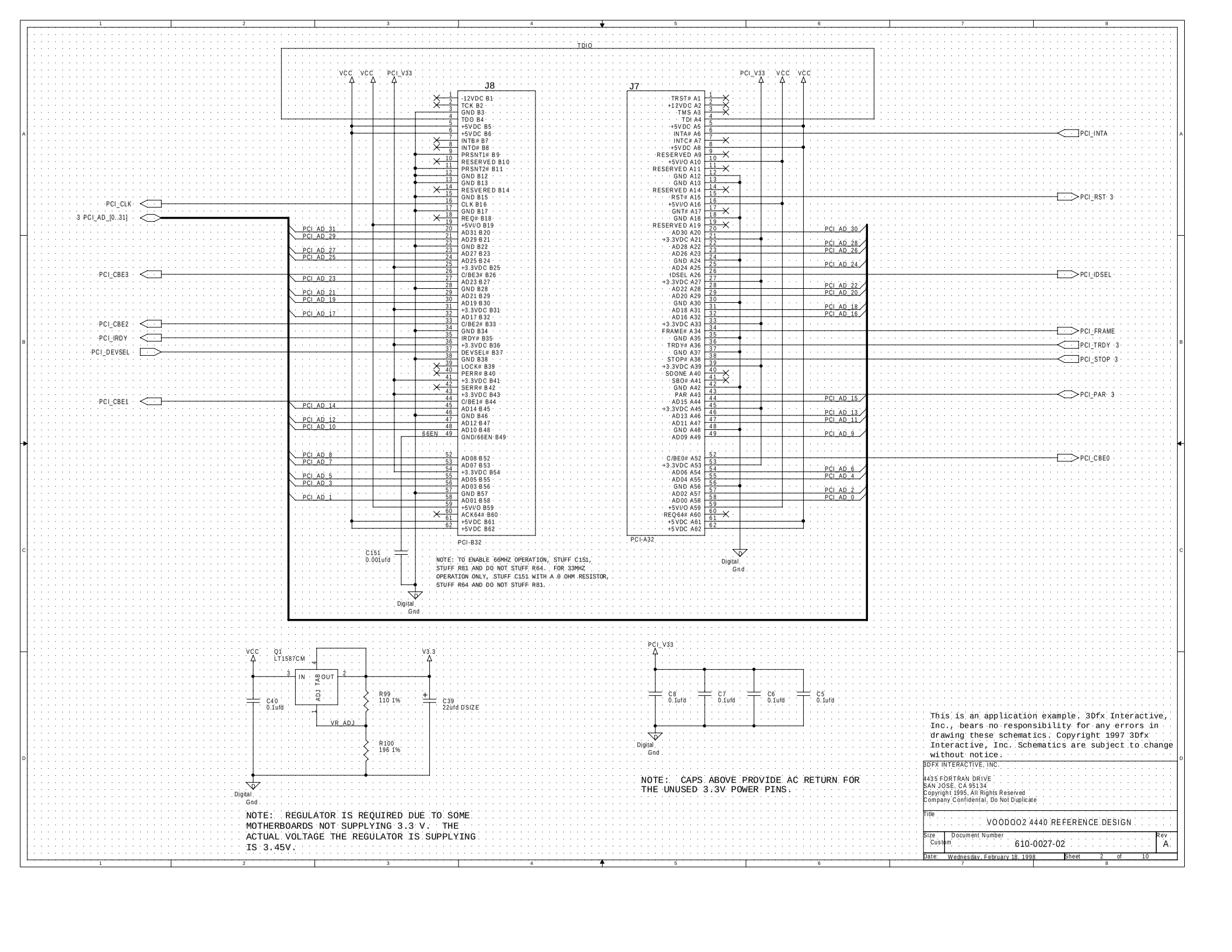

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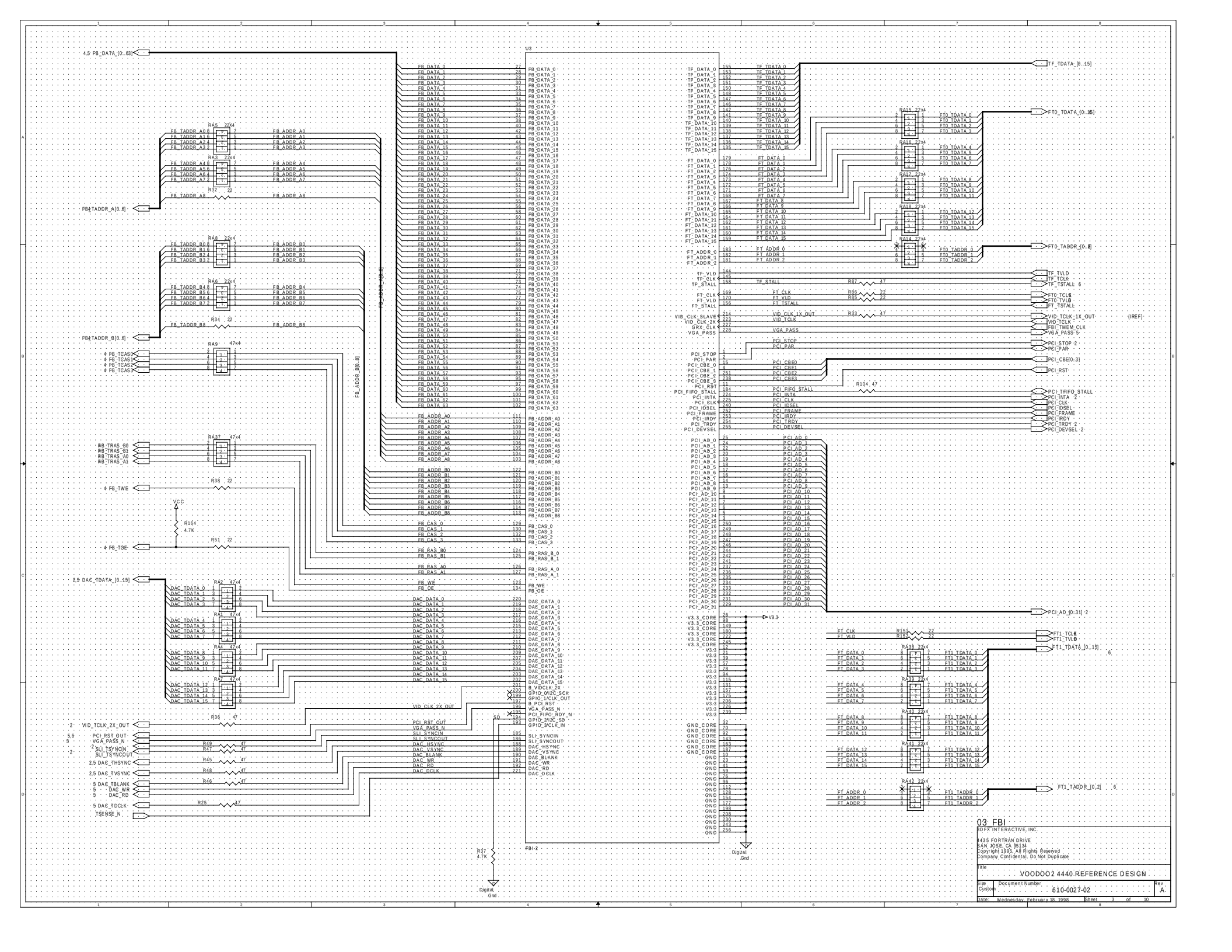
4.5 FB_DATA_[0..63]
FB4 TADDR_A[0..8]
FB4 TADDR_B[0..8]
4 FB_TCAS0
4 FB_TCAS1
4 FB_TCAS2
4 FB_TCAS3
4 FB_TRAS_B0
4 FB_TRAS_B1
4 FB_TRAS_A0
4 FB_TRAS_A1
4 FB_TWE
4 FB_TOE
2.5 DAC_TDATA_[0..15]
2 VID_TCLK_2X_OUT
5,6 PCI_RST_OUT
5 VGA_PASS_N
2 SLI_TSYNCIN
2 SLI_TSYNCOUT
2.5 DAC_THSYNC
2.5 DAC_TVSYNC
5 DAC_TBLANK
5 DAC_WR
5 DAC_RD
5 DAC_TDCLK
TSENSE_N
VCC
R164 4.7K
R37 4.7K
Digital Gnd
U3
FBI-2
TF_TDATA_[0..15]
FT0_TDATA_[0..15] 6
FT0_TADDR_[0..8] 6
TF_TVLD
TF_TCLK
TF_TSTALL 6
FT0_TCLK 6
FT0_TVLD 6
FT_TSTALL
VID_TCLK_1X_OUT
VID_TCLK
FBI_TMEM_CLK
VGA_PASS 5
PCI_STOP 2
PCI_PAR
PCI_CBE[0..3]
PCI_RST
PCI_TFIFO_STALL
PCI_INTA 2
PCI_CLK
PCI_IDSEL
PCI_FRAME
PCI_IRDY
PCI_TRDY 2
PCI_DEVSEL 2
PCI_AD[0..31] 2
V3.3
FT1_TCLK 6
FT1_TVLD 6
FT1_TDATA_[0..15] 6
FT1_TADDR_[0..2] 6
SD
03 FBI
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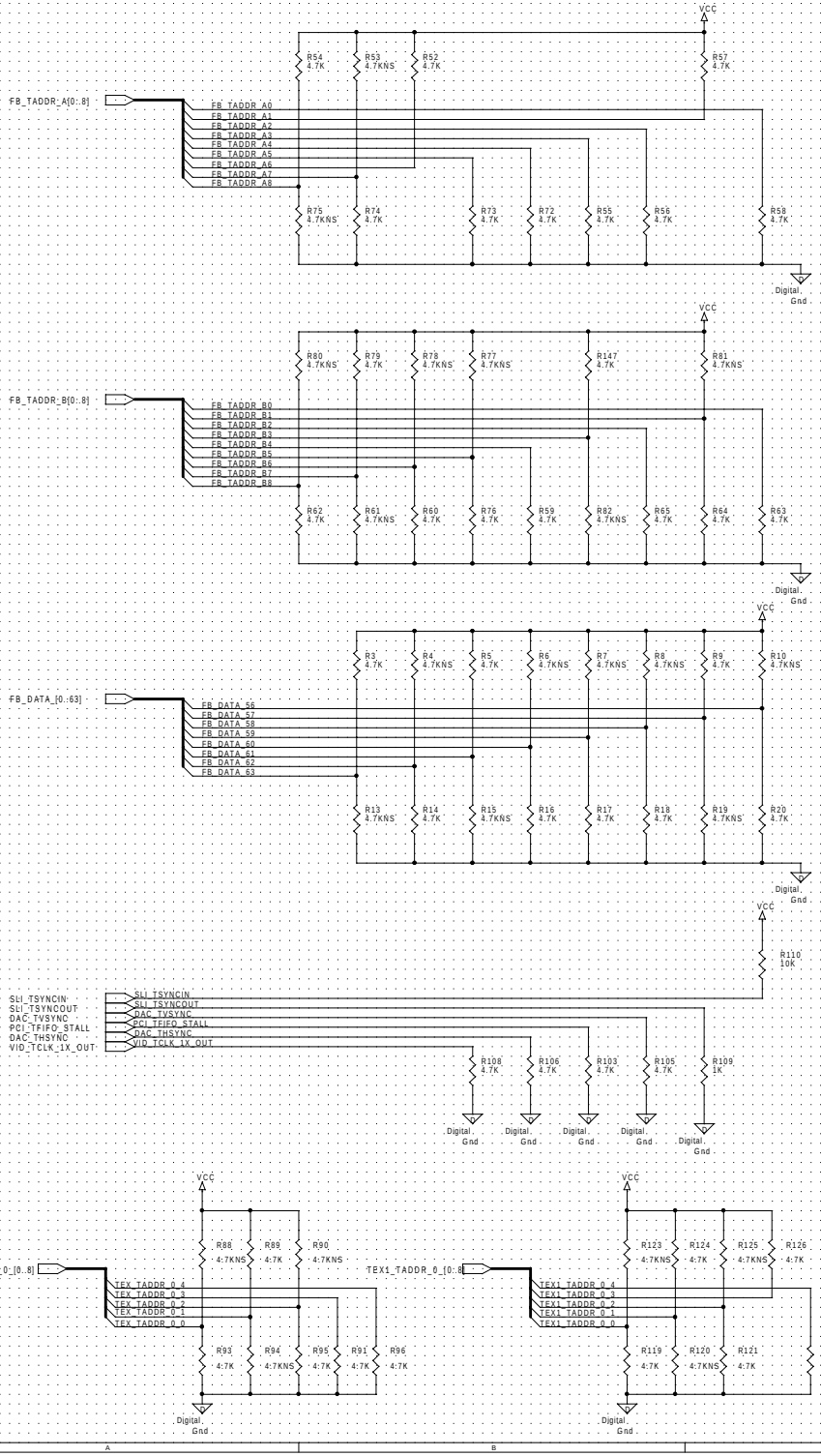

STRAPPING RESISTORS FBI-2

SIGNAL	DESCRIPTION
FB_ADDR_A0	PD REQUIRED TO SUPPORT LEGACY SOFTWARE MEMORY SPEED BIT 0
FB_ADDR_A1	PU REQUIRED TO SUPPORT LEGACY SOFTWARE MEMORY SPEED BIT 1
FB_ADDR_A2	PD REQUIRED TO SUPPORT LEGACY SOFTWARE GE BOARD ID
FB_ADDR_A3	VGA SHARED MEMORY BOARD (PD=PASSTHRU BOARD, PU= VGA SHARED MEMORY BOARD.)
FB_ADDR_A4	VGA_PASS PIN RESET VALUE
FB_ADDR_A5	HARDCODE PCI BASE ADDRES TO 0X10000000 (PD=NORMAL, PU=HARDCODE.)
FB_ADDR_A6	PCI CONFIG DEVICE TYPE (PD=DISPLAY, PU=MULTIMEDIA.)
FB_ADDR_A7	ENABLE PCI INTERRUPTS (PU=ENABLE), DEFAULT PD
FB_ADDR_A8	FAST PCI DEVICE (FAST DEVSEL TIMING, FAST BACK TO BACK CAPABLE, DEFUALT PU=FAST.)

FB_ADDR_B0	DISABLE PCI_STOP SIGNAL PIN FUNCTIONALITY (SETS DEFAULT STATE OF FBIINIT5[0].)
FB_ADDR_B1	DEVICE IS 66MHZ CAPABLE(PU) (SETS STATE OF PCI CONFIGURATION REGISTER STATUS[5].)
FB_ADDR_B2	DAC DATA OUTPUT PORT (PD=16 BIT, PU=24 BIT.)
FB_ADDR_B3	DEFAULT VALUE OF DAC_DATA[17]/GPIO_0/I2C_SCK WHEN POWERON FB_ADDR_B[2]=0, DEFAULT=PU
FB_ADDR_B4	DEFAULT VALUE OF DAC_DATA[18]/GPIO_1 WHEN POWERON FB_ADDR_B[2]=0
FB_ADDR_B5	BOARD ID, BIT 0, (4440 = 4), DEFAULT = PD
FB_ADDR_B6	BOARD ID, BIT 1 DEFAULT = PD
FB_ADDR_B7	BOARD ID, BIT 2 DEFAULT = PU
FB_ADDR_B8	BOARD ID, BIT 3 DEFAULT = PD

NOTE: THE EXACT MEMORY SPEED SHOULD BE DETERMINED BY VOLTAGE AND TEMPERATURE MARGIN TESTING YOUR DESIRED MEMORY MANUFACTURERS. THERE ARE DIFFERENCES IN OPERATING SPEED BETWEEN MANUFACTURERS AND SPEED GRADES. ALSO, ANY CHANGES TO THE REFERENCE BOARD ROUTE AND TERMINATION VALUES MAY IMPACT THE OPERATING SPEED.

FB_DATA_56	BOARD ID, BIT 4 DEFAULT = PD
FB_DATA_57	PCI DEVICE ID SELECT (PD= DEVICE 1, PU= DEVICE 2) DEFAULT = PU
FB_DATA_58	50+[CLOCK FREQ.] BIT 0, DEFAULT PD, 90MHZ
FB_DATA_59	50+[CLOCK FREQ.] BIT 1, DEFAULT PD, 90MHZ
FB_DATA_60	50+[CLOCK FREQ.] BIT 2, DEFAULT PD, 90MHZ
FB_DATA_61	50+[CLOCK FREQ.] BIT 3, DEFAULT PU, 90MHZ
FB_DATA_62	50+[CLOCK FREQ.] BIT 4, DEFAULT PD, 90MHZ
FB_DATA_63	50+[CLOCK FREQ.] BIT 5, DEFAULT PU, 90MHZ

SLI_SYNCIN	USED TO DETERMINE SLI HOOKUP (PU 10K)
SLI_SYNCOUT	USED TO DETERMINE SLI HOOKUP (PD 1K)
VSYNC	PREVENT FLOATING INPUT DURING POWERON
HSYNC	PREVENT FLOATING INPUT DURING POWERON
PCI_FIFO_STALL	PREVENT FLOATING INPUT DURING POWERON
VID_CLK_SLAVE	PREVENT FLOATING INPUT DURING POWERON

STRAPPING RESISTORS TMUs

TEX_ADDR_0_0	GENERAL PURPOSE, DEFAULT PD
TEX_ADDR_0_1	GENERAL PURPOSE, DEFAULT PU
TEX_ADDR_0_2	GENERAL PURPOSE, DEFUALT PD
TEX_ADDR_0_3	TMU ID 0, DEFAULT PD
TEX_ADDR_0_4	TMU ID 1, DEFAULT PD

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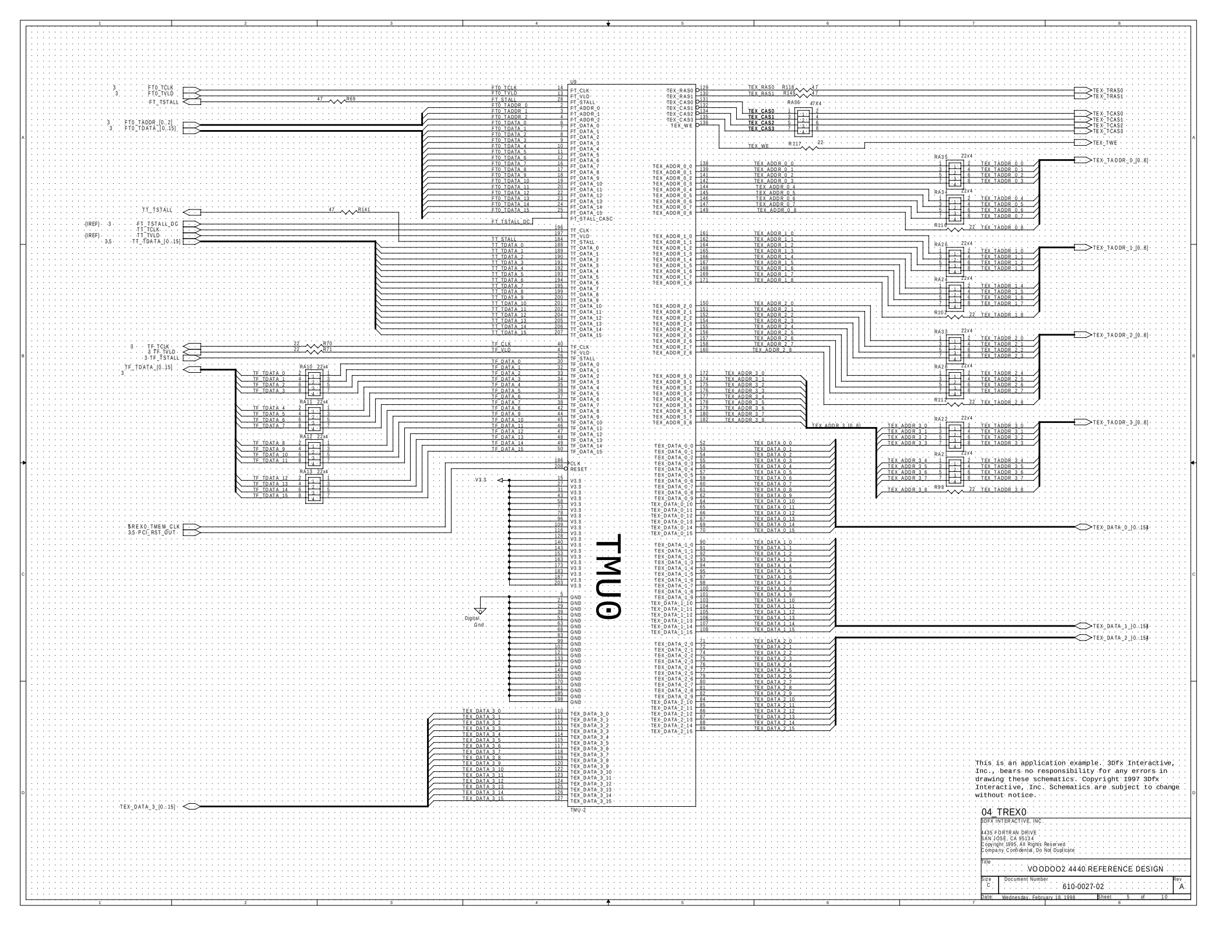

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04_TREX0

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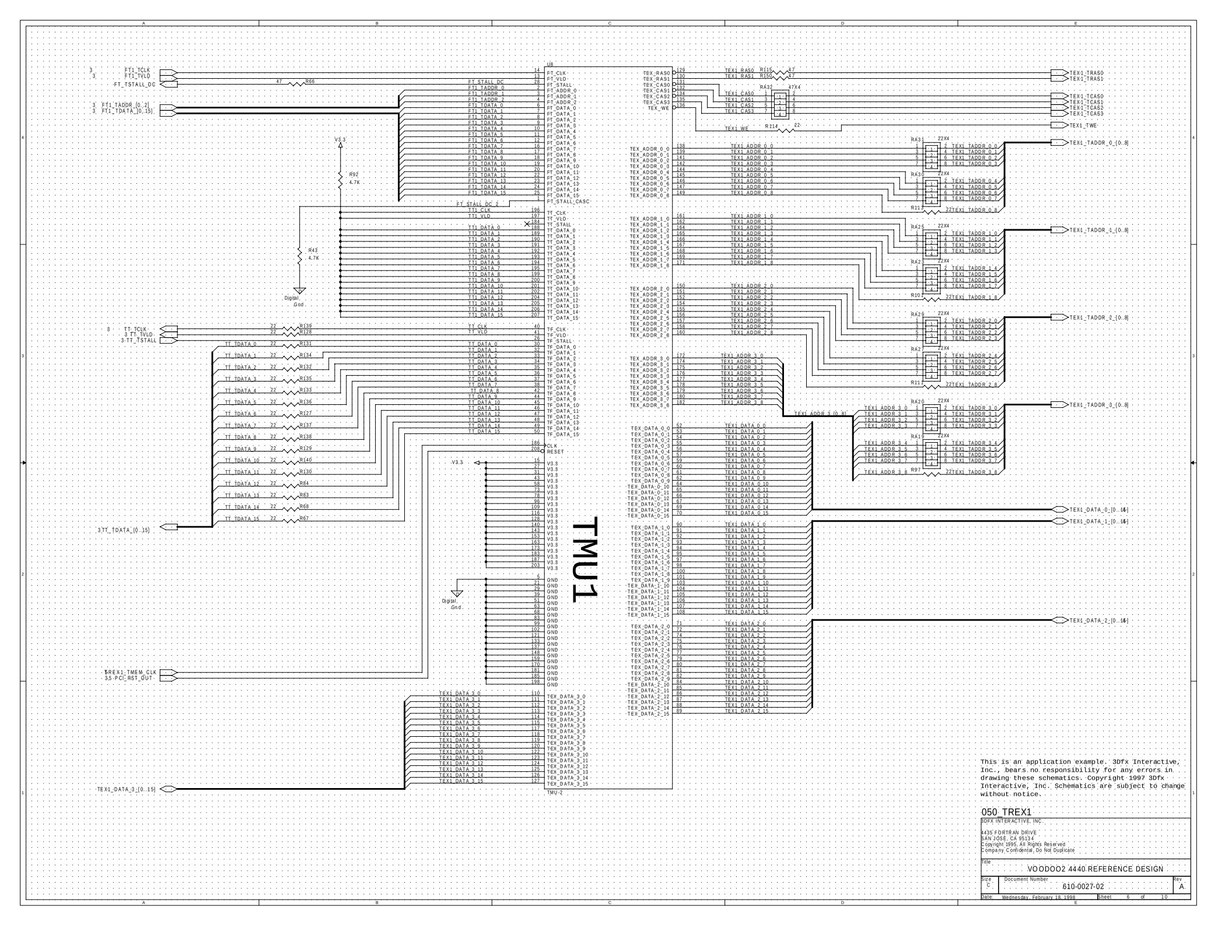

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050_TREX1

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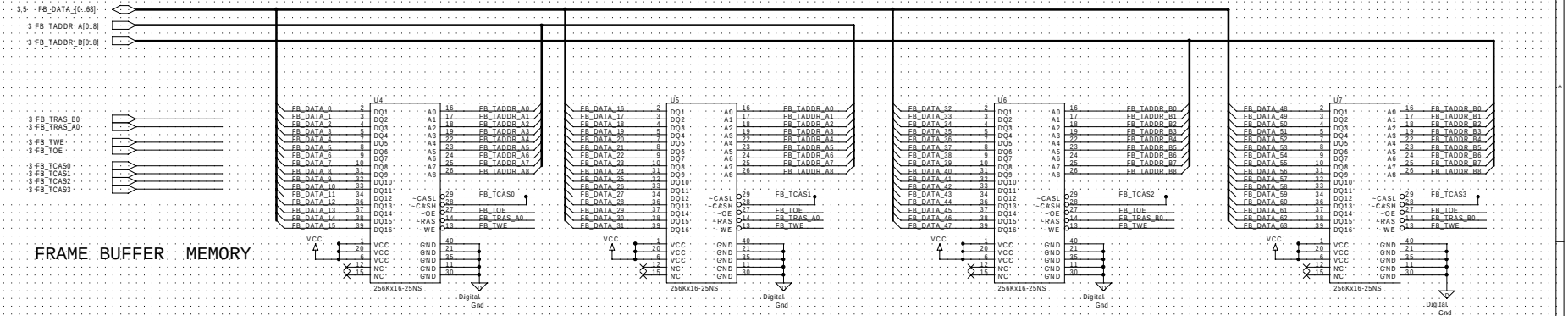
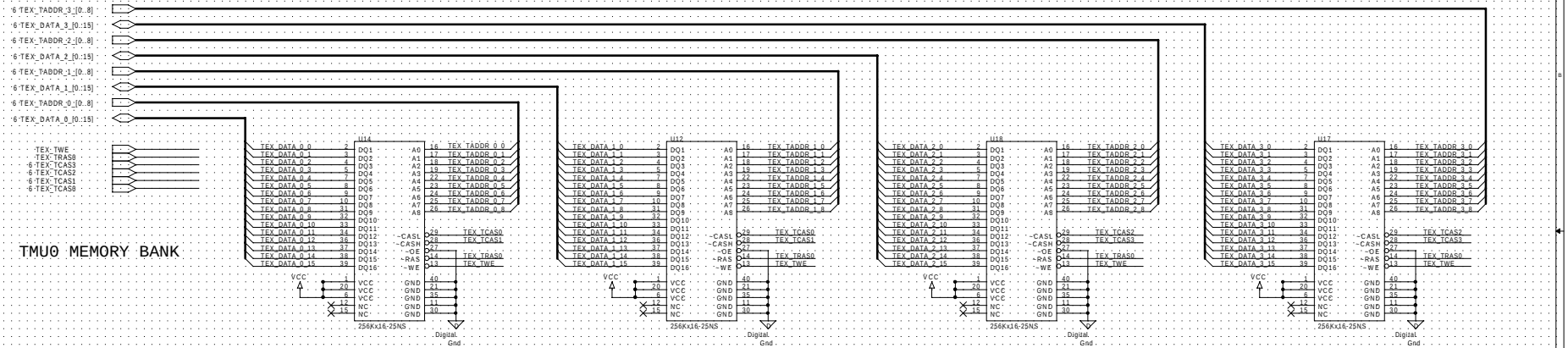
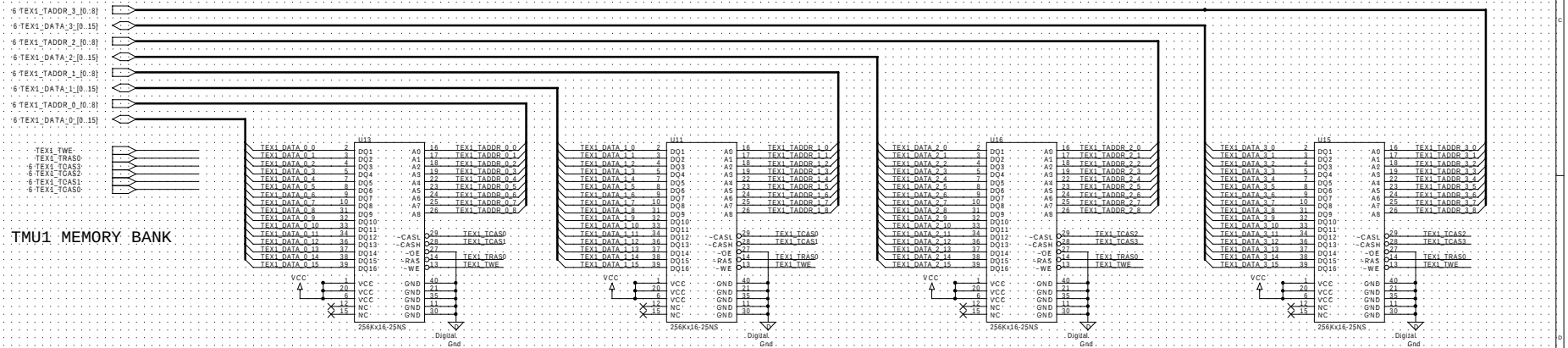
NOTE: Pins 11 and 30 are GND on Silicon Magic DRAMs. Every other DRAM manufacturer defines these pins as "true" NC, so they will not effect operation of non Silicon Magic DRAMs.



FRAME BUFFER MEMORY



TMU0 MEMORY BANK



TMU1 MEMORY BANK

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MEMORY.SCH

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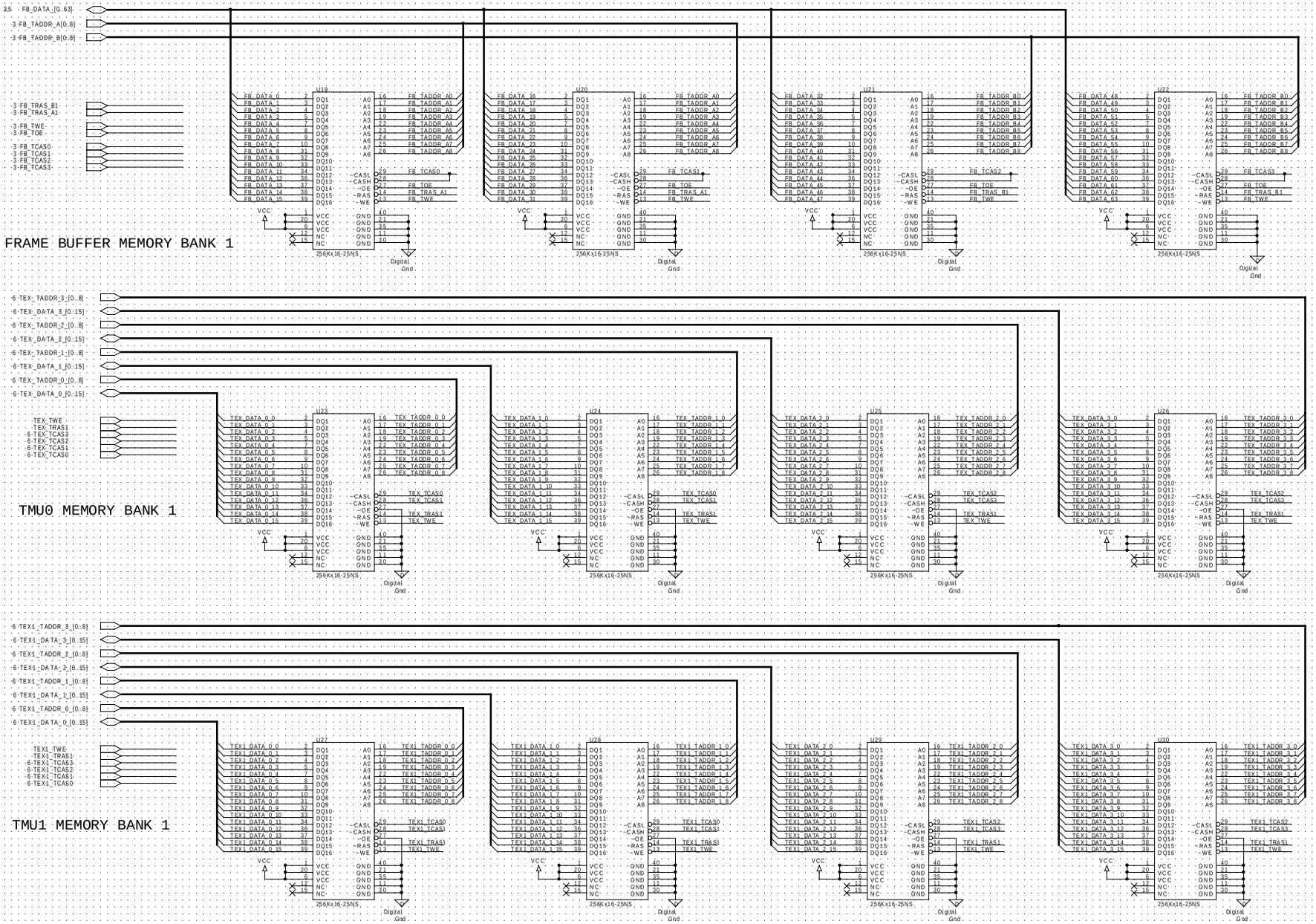
NOTE: Pins 11 and 30 are GND on Silicon Magic DRAMs. Every other DRAM manufacturer defines these pins as "true" NC, so they will not effect operation of non Silicon Magic DRAMs.



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NOTE: THE SLI INTERCONNECT CABLE SWAPS SLI_SYNCIN AND SLI_SYNCOUT BETWEEN THE BOARDS. THE 1K PULLDOWN ON DAC_DATA_0 IS PART OF THE BUFFER SWAPPING MECHANISM IN SLI MODE.

NOTE: LOOKING AT THE COMPONENT SIDE OF THE BOARD, PIN 1 OF J2 IS IN THE UPPER RIGHT OF THE 17X2 HEADER.

NOTE: DAISY CHAIN ALL SLI INTERCONNECT SIGNALS FROM FBI, DAC OR QUICKSWITCH TO J1.

NOTE: THE BUFFER FOR THE CLOCK NET MUST BE AN AC LOGIC FAMILY DEVICE. DO NOT USE ANY OTHER DEVICE SUCH AS F, ACT, ETC.

NOTE: PLACE R163 NEAR U1-50

NOTE: PLACE 75 OHM RESISTORS AS CLOSE AS POSSIBLE TO DAC, THEN PLACE VREF CAP AND RSET RESISTOR AS CLOSE AS POSSIBLE.

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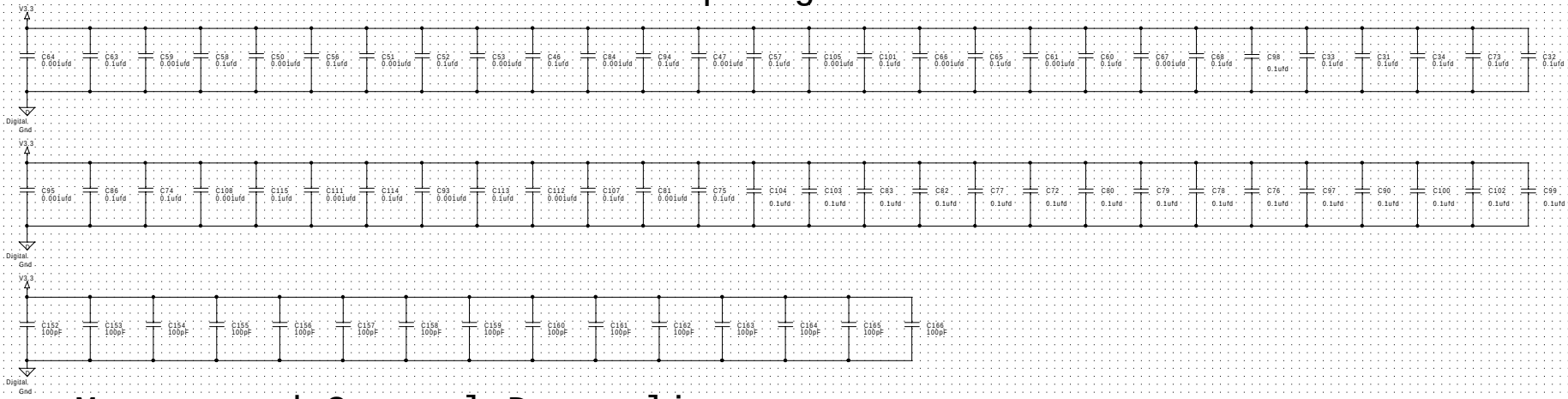
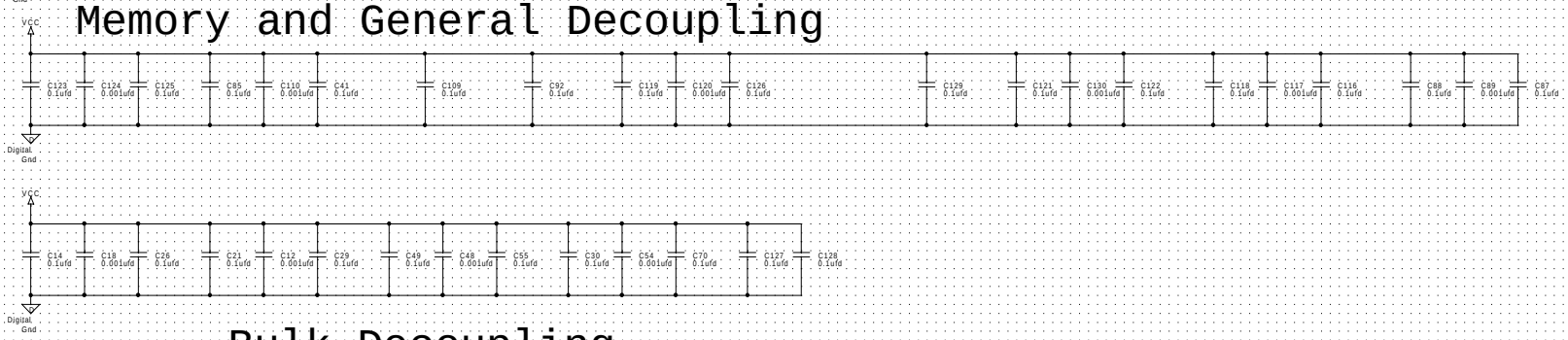
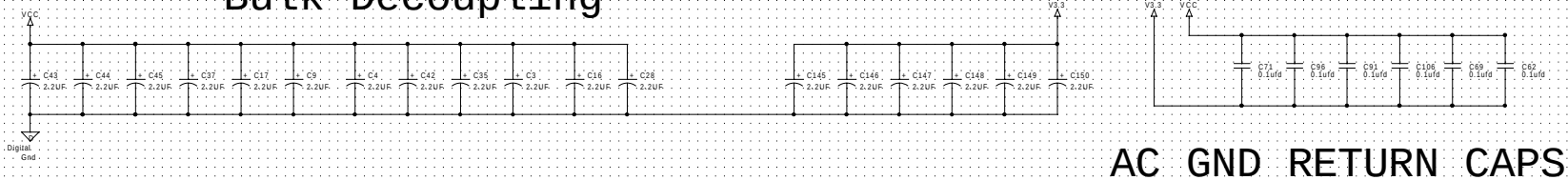
Voodoo2 3.3V VCC Decoupling



Memory and General Decoupling

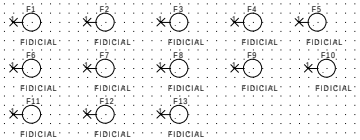


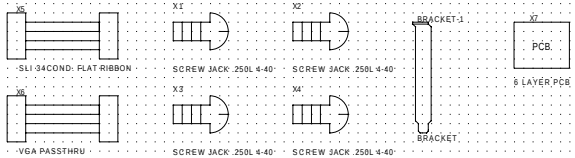
Bulk Decoupling

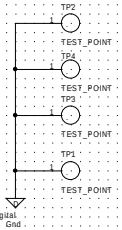


AC GND RETURN CAPS

BOARD AND ASIC FIDICIALS







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